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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,016	03/02/2004	Nobuhiko Akasaka	1081.1191	3571
<div>21171 7590 08/23/2007 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005</div>			<div>EXAMINER YANCHUS III, PAUL B</div>	
			<div>ART UNIT 2116</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 08/23/2007</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/790,016

Applicant(s)

AKASAKA

Examiner

Paul B. Yanchus

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 11-13 is/are rejected.
- 7) ☒ Claim(s) 8-10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 3/2/04, 3/27/06.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Kurd, US Patent no. 6,266,779.

Regarding claim 1, AAPA discloses a microcontroller operating in synchronization with a clock, comprising:

an arithmetic unit operating in synchronization with the clock [page 1, lines 18-21]; and

an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit which operates in synchronization with the clock [page 2, lines 7-18].

AAPA does not disclose a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock ($m \leq n$), and supplies the operation permission signal to the internal circuit of the internal resource, wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state. Kurd discloses a system resource prescaler [clock enable generator] which generates, from the clock, an operation permission signal [clock enable signal] denoting an operation permission state in m cycles out of n cycles of the clock [ratio], and supplies the operation permission signal to an internal circuit of

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an internal resource, wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state [Figure 1 and column 3, lines 35-38]. It would have been obvious to one of ordinary skill in the art to add the Kurd clock enable generator into the AAPA microcontroller to facilitate data transmission between resources which operate at different clock frequencies [Kurd, column 1, lines 38-49].

Regarding claim 2, AAPA further discloses that the bus interface of the internal resource operates in synchronization with the clock [page 2, lines 23-26].

Regarding claim 3, AAPA further discloses that the internal resource includes a communication macro controlling communication with outside, and an internal circuit of the communication macro includes a counter which generates a communication control clock [page 2, lines 10-18].

Regarding claim 3, AAPA further discloses that the internal resource comprises a pulse generation macro generating a control pulse, and an internal circuit of the pulse generation macro comprises a counter controlling a generation timing of the control pulse [page 2, lines 7-18].

Regarding claim 5, Kurd discloses that the clock enable generator is programmable to support a plurality of desired ratios [column 3, lines 25-38]. It is inherent that some type of register would be used to store the desired ratio.

Regarding claim 6, Kurd, as described above, discloses that the desired clock ratio of the clock enable generator is programmable. It would have been obvious to one of ordinary skill in the art that the ratio may be set to 1 to output an enable signal for every clock cycle.

Regarding claim 7, Kurd discloses that the clock enable generator dispersively allocates the m cycles throughout the n cycles [column 3, lines 25-38].

Regarding claim 11, AAPA discloses a a microcontroller operating in synchronization with a clock, comprising:

an arithmetic unit operating in synchronization with the clock [page 1, lines 18-21]; and

an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit which operates in synchronization with the clock [page 2, lines 7-18].

AAPA does not disclose a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock ($m \leq n$), and supplies the operation permission signal to the internal circuit of the internal resource, wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state. Kurd discloses a system resource prescaler [clock enable generator] which generates, from the clock, an operation permission signal [clock enable signal] denoting an operation permission state in m cycles out of n cycles of the clock [ratio], and supplies the operation permission signal to an internal circuit of an internal resource, wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state [Figure 1 and column 3, lines 35-38]. It would have been obvious to one of ordinary skill in the art to add the Kurd clock enable generator into the AAPA microcontroller to facilitate data transmission between resources which operate at different clock frequencies [Kurd, column 1, lines 38-49].

Regarding claim 12, Kurd further discloses that the operation permission signal is controlled to be set to the operation permission state on a cycle-by-cycle basis of the clock [column 3, lines 25-38].

Regarding claim 13, Kurd further discloses that the operation permission signal is set to the operation permission state in m cycles out of n cycles of the clock, and the values n and m can be set alterably [column 3, lines 25-38].

Allowable Subject Matter

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Byers et al., US Patent no. 5,394,443 discloses providing enable signals based on an input clock signal to a plurality of loads which operate in synchronization with the clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
August 19, 2007



REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
8/20/07